Listing of the claims:

This listing of claims replaces all prior versions.

1. (Currently Amended) A thin film Silicon on Insulator (SOI) device comprising:

a source;

a gate;

a drain;

an SOI layer;

a substrate layer configured and arranged, ~~wherein~~ when the substrate layer is maintained at a potential sufficiently lower than a potential of the source, to form a parasitic MOS channel ~~is formed~~ between the source and drain; and

a Deep N implant layer configured and arranged ~~formed between either the source or drain and the SOI layer~~ to prevent flow of current between the source and drain via the parasitic MOS channel when the device is in an off state.

2. (Currently Amended) The device of claim 1 wherein the Deep N implant layer is ~~formed~~ between the source and the SOI layer.

3. (Previously presented) The device of claim 1 wherein the Deep N implant layer is formed between the drain and the SOI layer.

4-11. (Cancelled).

12. (Currently Amended) The device of claim 1, wherein the substrate layer is configured and arranged to form the parasitic MOS channel when the substrate layer is maintained at a potential that is about 200 volts lower than the potential of the source.

13. (Previously presented) The device of claim 1, wherein the SOI layer has a thickness of about 1 micron.

14. (Previously presented) The device of claim 1, wherein the Deep N implant layer has a doping concentration about 1 order of magnitude higher than that of a gate region associated with the gate.

15. (Currently Amended) A thin film Silicon on Insulator (SOI) device comprising:

a source and a drain;

a gate between the source and the drain to control on and off states of the device;

a substrate layer;

a deep implant layer adjacent to at least one of ~~either~~ the source and ~~or~~ the drain; and

an SOI layer ~~disposed~~ between the substrate layer and the deep implant layer,

wherein, when the substrate layer is maintained at a potential sufficiently different than a potential of the source, the substrate layer forms a parasitic MOS channel ~~is formed~~ between the source and drain, and

wherein the deep implant layer prevents flow of current between the source and drain via the parasitic MOS channel when the device is in an off state.

16. (Currently Amended) The device of claim 15, wherein the deep implant layer is ~~formed~~ between the source and the SOI layer.

17. (Currently Amended) The device of claim 15, wherein the deep implant layer is ~~formed~~ between the drain and the SOI layer.

18. (Withdrawn) The device of claim 15, wherein the deep implant layer is a Deep P implant layer.

19. (Previously presented) The device of claim 15, wherein the deep implant layer is a Deep N implant layer.

20. (New) The device of claim 1, wherein

the SOI layer is on the substrate layer,

the implant layer is over a portion of the SOI layer that is in contact with the substrate layer and prevents current flow between the underlying substrate layer and at least one of a source and a drain over the implant layer.

21. (New) The device of claim 15, wherein

the SOI layer is on the substrate layer,

at least one of the source and the drain is over the implant layer, and

the implant layer prevents current flow between the at least one of the source and the drain and the underlying substrate layer.

22. (New) A thin film Silicon on Insulator (SOI) device comprising:

a substrate susceptible to parasitic MOS channel formation; and

a silicon layer on the substrate, the silicon layer including

a source,

a drain,

a deep implant region extending below and laterally adjacent at least one of the source and drain, and configured and arranged to prevent current flow between a parasitic MOS channel in the substrate and the at least one of the source and drain when the device is in an off state, and

a channel region above the deep implant region and between the source and drain.

23. (New) The device of claim 22, wherein the deep implant region has an implant concentration that is at least an order of magnitude higher than the concentration of gate, to prevent current flow between the parasitic MOS channel in the substrate and the at least one of the source and drain when the device is in an off state.